Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus comprising:

a first device to transmit a plurality of data signals in a parallel mode; and

a second device coupled to receive the plurality of data signals from the first device[[,]] ;

wherein the second device detects phase information of each data signal against a corresponding clock signal and feeds back the phase information to the first device, the first device adjusts an output delay of each data signal based on the phase information fed back from the second device and the second device feeds back the phase information of the first device in a serial mode.

2. (Canceled)

3. (Original) The apparatus of claim 1 wherein the second device samples parallel data patterns transmitted from the first device and feeds back the sampled data to the first device.

4. (Original) The apparatus of claim 3 wherein the second device samples the parallel data patterns in response to a first command signal from the first device.

5. (Original) The apparatus of claim 3 wherein the second device feeds back the sampled data to the first device in serial mode.

6. (Original) The apparatus of claim 1 wherein the first device

detects phase variations that are in excess of one bit of the sampled data fed back from the second device and shifts data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

7. (Currently Amended) An apparatus comprising:

a first device to transmit a plurality of data signals in a parallel format; and

a second device to receive the plurality of data signals from the first device,

wherein the second device detects phase information of each data signal with respect to a corresponding clock signal and adjusts a delay of the respective data signal based on the phase information detected prior to sampling of the data signals and the second device transmits parallel data sample to the first device, subsequent to the sampling of the data signals.

8. (Canceled)

9. (Currently Amended) The apparatus of claim ~~8~~ 7 wherein the first device, in response to receiving the parallel data sample from the second device, compares the parallel data sample to a programmed parallel data pattern.

10. (Original) The apparatus of claim 9 wherein the first device generates a signal to accompany data words being transmitted to the second device that match the programmed data pattern.

11. (Original) The apparatus of claim 10 wherein the second device, in response to the signal from the first device indicating a match to the programmed data pattern, recognizes phase variations that are in excess of one bit of the parallel data sample and shifts data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

12. (Currently Amended) A method comprising:

transmitting a plurality of data signals in parallel mode from a first device to a second device over a first bus;

detecting phase information of each data signal received at the second device against a corresponding clock signal;

sending the phase information from the second device to the first device, wherein the phase information is sent from the second device to the first device in a serial mode; and

adjusting an output delay of each data signal at the first device based on the phase information received from the second device.

13. (Canceled)

14. (Currently Amended) The method of claim 12 further including:

sampling and holding, at the second device, a parallel data pattern received from the first device;

feeding back the sampled data from the second device to the first device;

recognizing, at the first device, phase variations that are in excess of one bit of the sampled data fed back from the second device; and

shifting data bit positions between parallel words to align phase variations that are in excess of one bit interval.

15. (Currently Amended) A method comprising:

transmitting a plurality of data signals from a first device to a second device in a parallel mode over a first bus;

detecting, at the second device, phase information of each data signal with respect to a corresponding clock signal; ~~and~~

adjusting a delay of the respective data signal prior to sampling of the data signal at the second device[[.]];

sending a parallel data sample from the second device to the first device; and

upon receiving the parallel data sample at the first device, comparing the parallel data sample with a programmed parallel data pattern.

16. (Canceled)

17. (Currently Amended) The method of claim ~~16~~ 15 further including:

generating, from the first device, a signal to accompany data words being transmitted to the second device that match the programmed data pattern.

18. (Original) The method of claim 17 further including:

in response to the signal from the first device that indicates a match to the programmed data pattern, recognizing phase variations that are in excess of one bit of the parallel data sample; and

adjusting data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

19. (Currently Amended) A system comprising:

a processor;

a first component coupled to the processor; and

a second component coupled to the first component, wherein the first component transmits data words to the second component in parallel mode, each data word including a plurality of data bits, wherein the second component detects phase information of each data bit relative to a corresponding clock signal and feeds back the phase information of each data bit to the first component, the first component adjusts an output delay of each data bit based on the phase information fed back from the second component, wherein the second component samples parallel data patterns received from the first component and feeds back the sampled data patterns to the first component.

20. (Canceled)

21. (Currently Amended) The system of claim ~~20~~ 19 wherein the first component, based on the sampled data patterns fed back from the second component, recognizes phase variations that are in excess of one bit of the sampled data patterns fed back from the second component and adjust data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

22. (Original) The system of claim 19 wherein the first component receives data words from the second component in parallel mode, each data words including a plurality of data bits, and wherein the first component detects phase information of each data bit relative to a corresponding clock signal and adjusts a delay of the respective data bit based on the phase information detected prior to sampling of the data bits.

23. (Original) The system of claim 22 wherein the first component transmits parallel data sample to the second component subsequent to the sampling of the data bits.

24. (Original) The system of claim 23 wherein, upon receiving the parallel data sample from the first component, the second component compares the parallel data sample to a programmed parallel data pattern and generates a signal to accompany data words being transmitted to the first component that match the programmed data pattern.

25. (Currently Amended) A machine-readable medium comprising instructions which, when executed by a machine, cause the machine to perform operations including:

transmitting a plurality of data signals in parallel mode from a first device to a second device over a first bus;

detecting phase information of each data signal received at the second device against a corresponding clock signal;

sending the phase information from the second device to the first device; ~~and~~

adjusting an output delay of each data signal at the first device based on the phase information received from the second device[[.]];

sampling and holding, at the second device, a parallel data pattern received from the first device;

feeding back the sampled data from the second device to the first device;

recognizing, at the first device, phase variations that are in excess of one bit of the sampled data fed back from the second device; and

shifting data bit positions between parallel words to align phase variations that are in excess of one bit interval.

26. (Canceled)

27. (Currently Amended) The machine-readable medium of claim ~~26~~ 25 wherein the operations performed further including:

transmitting a plurality of data signals from the second device to the first device in parallel mode;

detecting, at the first device, phase information of each data signal with respect to a corresponding clock signal; and

adjusting a delay of the respective data signal prior to sampling of the data signal at the first device.

28. (Original) The machine-readable medium of claim 27 wherein the operations performed further including:

sending parallel data sample from the first device to the second device; and

upon receiving the parallel data sample at the second device, comparing the parallel data sample with a programmed parallel data pattern.

29. (Original) The machine-readable medium of claim 28 wherein the operations performed further including:

generating, from the second device, a signal to accompany data words being transmitted to the first device that match the programmed data pattern.

30. (Original) The machine-readable medium of claim 29 wherein the operations performed further including:

in response to the signal from the second device that indicates a match to the programmed data pattern, recognizing phase variations that are in excess of one bit of the parallel data sample; and

adjusting, at the first device, data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

31. (New) An apparatus comprising:

a first device to transmit a plurality of data signals in a parallel mode; and

a second device coupled to receive the plurality of data signals from the first device;

wherein the second device detects phase information of each data signal against a corresponding clock signal and feeds back the phase information to the first device, the first device adjusts an output delay of each data signal based on the phase information fed back from the second device and the second device samples parallel data patterns transmitted from the first device and feeds back the sampled data to the first device.

32. (New) The apparatus of claim 31 wherein the second device samples the parallel data patterns in response to a first command signal from the first device.

32. (New) The apparatus of claim 31 wherein the second device feeds back the sampled data to the first device in serial mode.

33. (New) The apparatus of claim 31 wherein the second device feeds back the phase information to the first device in serial mode.

34. (New) An apparatus comprising:

a first device to transmit a plurality of data signals in parallel mode; and

a second device coupled to receive the plurality of data signals from the first device,

wherein the second device detects phase information of each data signal against a corresponding clock signal and feeds back the phase information to the first device, the first device adjusts an output delay of each data signal based on the phase information fed back from the second device; and

wherein the first device detects phase variations that are in excess of one bit of the sampled data fed back from the second device and shifts data bit positions between parallel data words to align phase variations that are in excess of one bit interval.

35. (New) The apparatus of claim 34 wherein the second device feeds back the phase information to the first device in serial mode.

36. (New) The apparatus of claim 34 wherein the second device samples parallel data patterns transmitted from the first device and feeds back the sampled data to the first device.

37. (New) A method comprising:

transmitting a plurality of data signals in parallel mode from a first device to a second device over a first bus;

detecting phase information of each data signal received at the second device against a corresponding clock signal;

sending the phase information from the second device to the first device;

adjusting an output delay of each data signal at the first device based on the phase information received from the second device;

sampling and holding, at the second device, parallel data pattern received from the first device;

feeding back the sampled data from the second device to the first device;

recognizing, at the first device, phase variations that are in excess of one bit of the sampled data fed back from the second device; and

shifting data bit positions between parallel words to align phase variations that are in excess of one bit interval.

38. (New) A system comprising:

a processor;

a first component coupled to the processor; and

a second component coupled to the first component, wherein the first component transmits data words to the second component in parallel mode, each data word including a plurality of data bits, wherein the second component detects phase information of each data bit relative to a corresponding clock signal and feeds back the phase information of each data bit to the first component, the first component adjusts an output delay of each data bit based on the phase information fed back from the second component;

wherein the first component receives data words from the second component in a parallel mode, each data words including a plurality of data bits, and wherein the first component detects phase information of each data bit relative to a corresponding clock signal and adjusts a delay of the respective data bit based on the phase information detected prior to sampling of the data bits.

39. (New) The system of claim 38 wherein the first component transmits parallel data sample to the second component subsequent to the sampling of the data bits.

40. (New) The system of claim 39 wherein, upon receiving the parallel data sample from the first component, the second component compares the parallel data sample to a programmed parallel data pattern and generates a signal to accompany data words being transmitted to the first component that match the programmed data pattern.